Monolithic Integration of AlGaAs/GaAs HBT and GaAs Junction-Gate Floated Electron Channel Field Effect Transistor Using Selective MOCVD Growth

Hyunchol Shin, Jeong-Hwan Son, and Young-Se Kwon

Abstract— **A novel GaAs BiFET structure based on AlGaAs/GaAs HBT and GaAs junction-gate floated electron channel field effect transistor (J-FECFET) has been developed. Selective metalorganic chemical vapor deposition (MOCVD) growth is extensively used for the BiFET. Structural advantage of the BiFET is that the epitaxial layers of J-FECFET is identical with the lower part of a conventional heterojunction bipolar tranistor (HBT). Transconductance of the fabricated J-FECFET with $1 \times 200\,\mu m^2$ gate is 102 mS/mm with f_T and f_{MAX} of 10.7 GHz and 27.3 GHz, respectively. DC current gain of HBT is 21 at a collector current density of 50 KA/cm^2 with emitter area of $3 \times 2\,\mu m^2$. The new integration technology offer a foundation for development of various multifunction monolithic microwave integrated circuits (MMIC's).**

I. Introduction

MONOLITHIC integration of heterojunction bipolar transistors (HBT's) and field effect transistors (FET's) on the same substrate, which is called a BiFET technology, is one of the most challenging issues of multifunction microwave circuit applications. HBT's have high current driving capability, high switching speed and low $1/f$ noise. On the other hand, FET's have high input impedance and low noise characteristics. Because of these supplemental relationships of HBT's and FET's, GaAs BiFET technology is expected to be a breakthrough in the fields of GaAs multifunction monolithic microwave integrated circuits (MMIC's).

Previous attempts on monolithic integration of HBT and FET have relied on either a selective-area regrowth technique [1], or a stacked epitaxial structure with the FET channel merged into the HBT emitter layer [2] or under the HBT collector layer [3]. Recently, a fully functional MMIC circuit integrating HBT's, HEMT's, and p-i-n diodes using selective MBE growth has been reported [4].

In this letter, we report a novel BiFET structure integrating a conventional AlGaAs/GaAs HBT with a junction-gate floated electron channel field effect transistor (J-FECFET) [5]. J-FECFET features a triangular void over SiO_2 stripe formed by selective MOCVD growth. An effective short channel length independent of the metallized gate length is obtained because the distance between the n^+ ohmic layers separated by a void is very short. The thick n^+ layers of source and drain lead to a very small parasitic series resistance. The parasitic gate capacitance is much lower than that of the conventional JFET. With those advantages, monolithic integration of the J-FECFET with a conventional HBT will provide a novel BiFET technology with simple fabrication process and high performance capabilities.

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H. Shin, and Y.-S. Kwon are with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, 373-1 Kusong-dong, Yusong-gu, Taejon, 305-701, Korea.

J.-H. Son is with LG Semicon Co. Ltd., 1 Hyangjeong-dong, Hungduk-gu, Cheongju, 360-480, Korea.

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II. Device Structure and Fabrication

The device structure is shown in Fig. 1, which is composed of a conventional HBT and a J-FECFET. The subcollector (n^+ GaAs), collector (n^- GaAs) and base (p^+ GaAs) layers in HBT are exactly matched with the ohmic (n^+ GaAs), active channel (n^- GaAs) and junction-gate(p^+ GaAs) layers in J-FECFET, respectively. Hence, the HBT and J-FECFET can be integrated without any modifications to their own structures. The epitaxial layer structure used in this work is shown in Table I, which also describes how the epi-layers are shared by the two different devices. In J-FECFET, carriers are flowed from the source end to the drain end of the thick n^+ layer and modulated by the depletion of the junction gate. The maximum current density of J-FECFET is, therefore, determined by the channel thickness and the doping concentration in the active channel layer which is also a collector layer of HBT. The collector layer is chosen to be 5×10^{16} cm^{-3}—doped and 7000 Å—thick considering the HBT operation. Thus, the doping concentration in the channel layer of J-FECFET is also 5×10^{16} cm^{-3}. The channel thickness of J-FECFET can be varied by changing the SiO_2 stripe width because the void height is proportional to the stripe width. The stripe width is chosen to be 2.0 μm by simple calculation to provide approximately 200 mA/mm of maximum current density.

The fabrication process is as follows. The SiO_2 stripes were formed on (001) GaAs substrate using e-beam evaporation and lift-off process. An atmospheric-pressure MOCVD was employed to grow the epitaxial structure. It has been experimentally proved [7] that the geometrical shapes of the laterally grown facets during selective MOCVD exhibit four different types depending on the growth parameters. Growing in this work was performed under the condition of a reverse mesa

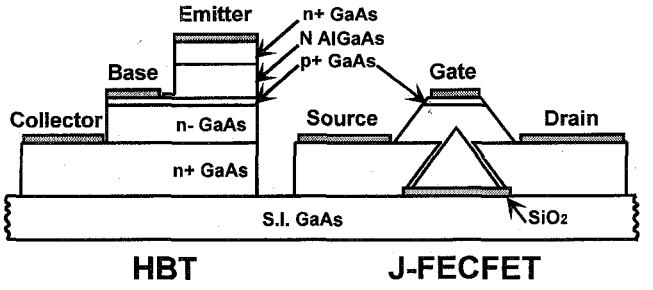

Fig. 1. Cross section of the BiFET structure integrating a conventional AlGaAs/GaAs HBT and a GaAs junction-gate floated electron channel FET, which shows that base and collector layers of HBT are shared with gate and channel layers of J-FECFET, respectively.

TABLE I
EPITAXIAL LAYER STRUCTURE OF BiFET GROWN BY MOCVD

Material	Thickness (Å)	Doping (cm^{-3})	Growth Temp. (°C)	Layers	
				HBT	J-FECFET
n^+-GaAs	800	Si 5×10^{18}	700	Emitter Cap.	
N-$Al_{0.3}Ga_{0.7}As$	1500	Si 1×10^{18}	700	Emitter	
p^+-GaAs	1000	C 2×10^{19}	650	Base	Gate
n-GaAs	7000	Si 5×10^{16}	650	Collector	Channel
n^+-GaAs	5000	Si 5×10^{18}	650	Sub-collector	Ohmic

shape. The wafer was thermally cleaned at 700°C for 20 min under AsH_3 overpressure before growth. Emitter metal evaporation and emitter edge thinning [7] were performed after selective MOCVD growth. Collector, source, and drain contact-areas were formed by wet etching. Device isolation was then achieved by etching a mesa down to the semi-insulating substrate. 2500 Å SiO_2 was sputter-deposited right after the isolation etching in order that the gate metal should not be contacted to the n^+ ohmic layer in the mesa edge. All ohmic metals for the base and collector contacts in HBT as well as the source, drain and gate contacts in J-FECFET were evaporated with AuGe/Ni/Au and then alloyed simultaneously at 430°C. Gold electroplating was finally performed for interconnection. Fig. 2 shows the photograph of the fabricated devices. The photograph clearly exhibits that HBT's and J-FECFET's are successfully integrated on the same substrate.

III. RESULTS AND DISCUSSIONS

The devices resulting from the monolithic integration of HBT's and J-FECFET's on the same substrate were successfully fabricated and measured. Fig. 3 shows the I–V characteristics of J-FECFET. The metal gate width and length are $2 \times 100\,\mu$m and 1 μm, respectively, but the junction-gate length of the p^+ layer is slightly larger than 1 μm. A maximum extrinsic transconductance of 102 mS/mm was obtained at a drain current density of 200 mA/mm. Threshold voltage was −2.8 V. Very low knee voltage of about 0.7 V implies a low parasitic source resistance as mentioned earlier. The high-

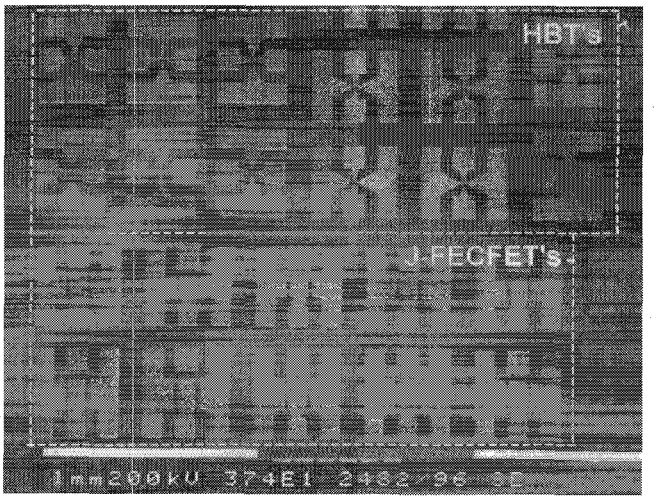

Fig. 2. Photograph of the fabricated BiFET.

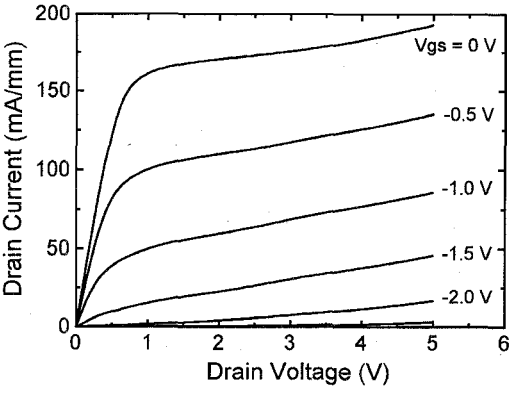

Fig. 3. Output characteristics of the fabricated J-FECFET with 200 μm of gate width and 1 μm of gate length. Maximum g_m is 102 mS/mm at V_{DS} = 3 V.

frequency characteristics were also measured on wafer using Wiltron 360 B vector network analyzer. The current gain cut off frequency (f_T) and the maximum oscillation frequency (f_{MAX}) were 10.5 GHz and 27.3 GHz, respectively, at V_{DS} = 3 V and I_{DS} = 100% of I_{DSS}. The comparable f_T with a conventional MESFET is attributed to the relatively small parasitic gate-to-source capacitance C_{gs} of 0.29 pF. The low value of C_{gs} is due to the low doping concentration in the channel layer.

Fig. 4 shows the common emitter I–V characteristics of HBT with emitter area of $3 \times 2\,\mu m^2$. The DC current gain is 21 at a collector current density of 50 KA/cm^2. Specific contact resistance of the base metal is $1.2 \times 10^{-5}\,\Omega\,cm^2$. Offset voltage and ohmic linearity are poor because the alloy process is not optimized yet. Further improvement of the HBT performance is expected by adopting a self-align process and nonalloyed ohmic contact metals.

IV. CONCLUSION

We have presented the fabrication of a new GaAs BiFET structure which employs a conventional AlGaAs/GaAs HBT and a GaAs J-FECFET. Selective MOCVD growth on a

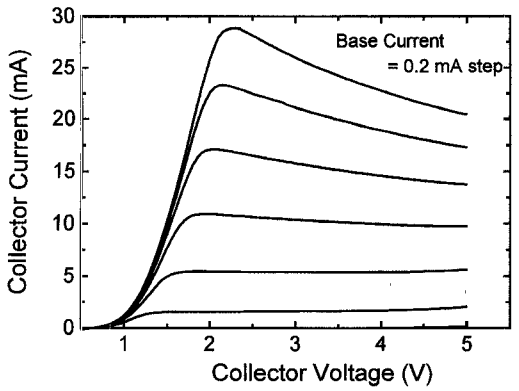

Fig. 4. Common-emitter characteristics of the fabricated HBT with $3 \times 2\,\mu m^2$ emitter area, for a base current step of 200 μA. DC current gain is 21 at a collector current density of 50 KA/cm^2.

patterned substrate was used for the BiFET structure. J-FECFET has the same epitaxial structure with the lower part of a conventional HBT, which makes it possible to directly combine the two devices without any structural modifications. Those structural advantages of this BiFET lead to relatively simple fabrication process compared to previously reported HBT/FET integration techniques. The fabricated devices have shown good performance and it is possible to apply the proposed BiFET structure to multifunction MMIC's.

REFERENCES

[1] D. C. Streit, D. K. Umemoto, T. R. Block, A. Han, M. Wojtowicz, K. Kobayashi, and A. K. Oki, "Selective molecular beam epitaxy for multifunction microwave integrated circuits," in *Int. Symp. Compound Semiconductor,* 1994, pp. 685–688.

[2] D. Cheskis, C. E. Chang, W. H. Ku, P. M. Asbeck, M. F. Chang, R. L. Pierson, and A. Sailer, "Co-integration of GaAlAs/GaAs HBT's and GaAs FET's with a simple, manufacturable process," in *IEDM Tech. Dig.,* 1992, pp. 91–94.

[3] K. Itakura, Y. Shimamoto, T. Ueda, S. Katsu, and D. Ueda, "A GaAs Bi-FET technology for large scale integration," in *IEDM Tech. Dig.,* 1989, pp. 389–392.

[4] K. W. Kobayashi, D. C. Streit, D. K. Umemoto, and A. K. Oki, "A novel monolithic HBT-p-i-n-HEMT integrated circuit with HBT active feedback and p-i-n diode variable gain amplifier," *IEEE Trans. Microwave Theory Tech.,* vol. 43, no. 5, pp. 1004–1009, May 1995.

[5] C. T. Kim, Y. J. Lee, and Y. S. Kwon, "A GaAs junction-gate FECFET (J-FECFET) for digital integrated circuits," *Jpn. J. Appl. Phys.,* vol. 32, no. 1B, pp. 556–559, Jan. 1993.

[6] H. Asai and S. Ando, "Lateral growth process of GaAs over Tungsten gratings by metalorganic chemical vapor deposition," *J. Electrochem. Soc.,* vol. 132, no. 10, pp. 2445–2453, Oct. 1985.

[7] H. Lin and S. Lee, "Super-gain AlGaAs/GaAs heterojunction bipolar transistor using an emitter edge thinning design," *Appl. Phys. Lett.,* vol. 47, no. 8, pp. 839–841, 1985.